WHAT IS CLAIMED IS:

1. A circuit, comprising:

a switch configured to receive a synchronizing signal having an active state, and an inactive state, wherein the switch has an on state activated by the active state and deactivated by the inactive state; and

a current path coupled to the switch, wherein the current path is configured to pass a current when the on state is deactivated, and wherein the switch is configured to pass the current when the on state is activated.

2. The circuit of claim 1, wherein the switch includes a bipolar junction transistor and the current path includes a pair of diodes, and wherein a cathode of a selected one of the pair of diodes is coupled to the switch.

3. The circuit of claim 2, further comprising:

a resistor coupled between a voltage supply and an anode of each one of the pair of diodes, wherein the resistor has a value selected so that a magnitude of a current flowing from the voltage supply through the resistor is always greater than a magnitude of a sink current coupled to the switch.

4. The circuit of claim 1, wherein the switch and the current path are included in a single metal oxide semiconductor field effect transistor.

5. The circuit of claim 1, further comprising:

a capacitor coupled to the switch and the current path, wherein the capacitor is coupled to an integrated circuit pin configured to source and sink the current.

6. The circuit of claim 1, wherein the current path includes a voltage clamping circuit.

7. A circuit, comprising:

an oscillator having a current source-sink connection;

a switch coupled to the current source-sink connection and configured to receive a synchronizing signal having an active state, and an inactive state, wherein the switch has an on state activated by the active state and deactivated by the inactive state; and

a current path coupled to the switch, wherein the current path is configured to pass a current when the on state is deactivated, and wherein the switch is configured to pass the current when the on state is activated.

8. The circuit of claim 7, wherein the switch is coupled to the current source-sink connection using a capacitor.

9. The circuit of claim 7, wherein the oscillator is included in a pulse width modulator.

10. The circuit of claim 9, further comprising:

a self-oscillating, push-pull switching circuit coupled to the oscillator.

11. The circuit of claim 10, wherein the self-oscillating, push-pull switching circuit is a Royer-class converter.

12. The circuit of claim 10, further comprising:

at least one cold-cathode fluorescent lamp coupled to the self-oscillating, push-pull switching circuit.

13. A computer, comprising:

a processor;

at least one cold-cathode fluorescent lamp capable of being communicatively coupled to the processor;

an oscillator having a current source-sink connection;

a switch coupled to the current source-sink connection and configured to receive a synchronizing signal having an active state and an inactive state, wherein the switch has an on state activated by the active state and deactivated by the inactive state;

a current path coupled to the switch, wherein the current path is configured to pass a current when the on state is deactivated, and wherein the switch is configured to pass the current when the on state is activated; and

a self-oscillating, push-pull switching circuit coupled to the oscillator and to the at least one cold-cathode fluorescent lamp.

14. The computer of claim 13, further comprising:

a global positioning system receiver capable of being communicatively coupled to the processor.

15. The computer of claim 14, further comprising:

a display capable of being communicatively coupled to the processor and lighted by the at least one cold-cathode fluorescent lamp.

16. A method of adjusting the operation of an oscillator, comprising:

connecting a first capacitor to a timing input of the oscillator;

connecting a switch to the first capacitor;

activating the switch using a synchronizing signal in a first state to pass a current from the timing input through the switch to charge the first capacitor,

wherein a cycle of the synchronizing signal is shorter than a free-running cycle of an oscillation signal of the oscillator; and

deactivating the switch using the synchronizing signal in a second state to pass the current through a second capacitor.

17. The method of claim 16, wherein the first capacitor is a physical capacitor and the second capacitor is a stray capacitance associated with the switch.

18. The method of claim 16, wherein the switch includes a transistor.

19. The method of claim 18, wherein the synchronizing signal in the first state places the transistor in a saturated mode of operation.

20. A method of operating a power converter, comprising:

coupling an oscillator to a power converter;

coupling a first capacitor to a timing input of the oscillator;

charging the first capacitor using a current which flows out of the timing input;

adding a second capacitor in series with the first capacitor to change the charging time of a series combination of the first and second capacitors to be shorter than a charging time of the first capacitor; and

discharging the first and second capacitors using a current which flows into the timing input.

21. The method of claim 20, wherein charging the first capacitor using a current which flows out of the timing input further comprises:

coupling a switch to the first capacitor; and

activating the switch to charge the first capacitor using a synchronizing signal in a first state, the synchronizing signal having a cycle which is shorter than a cycle of an oscillation signal of the oscillator.

22. The method of claim 21, wherein adding a second capacitor in series with the first capacitor to change the charging time of a series combination of the first and second capacitors further comprises:

deactivating the switch to charge the series combination of the first and second capacitors, wherein the second capacitor is a stray capacitance associated with the switch.

23. The method of claim 21, wherein discharging the first capacitor using a current which flows into the timing input further comprises:
deactivating the switch using the synchronizing signal in a second state.

24. The method of claim 23, wherein a time period during which the synchronizing signal is in the second state is substantially less than a time period during which the synchronizing signal is in the first state.

25. The method of claim 23, wherein a sum of a time period during which the synchronizing signal is in the second state and a time period during which the synchronizing signal is in the first state is less than a time period of a cycle of an oscillation signal of the oscillator.